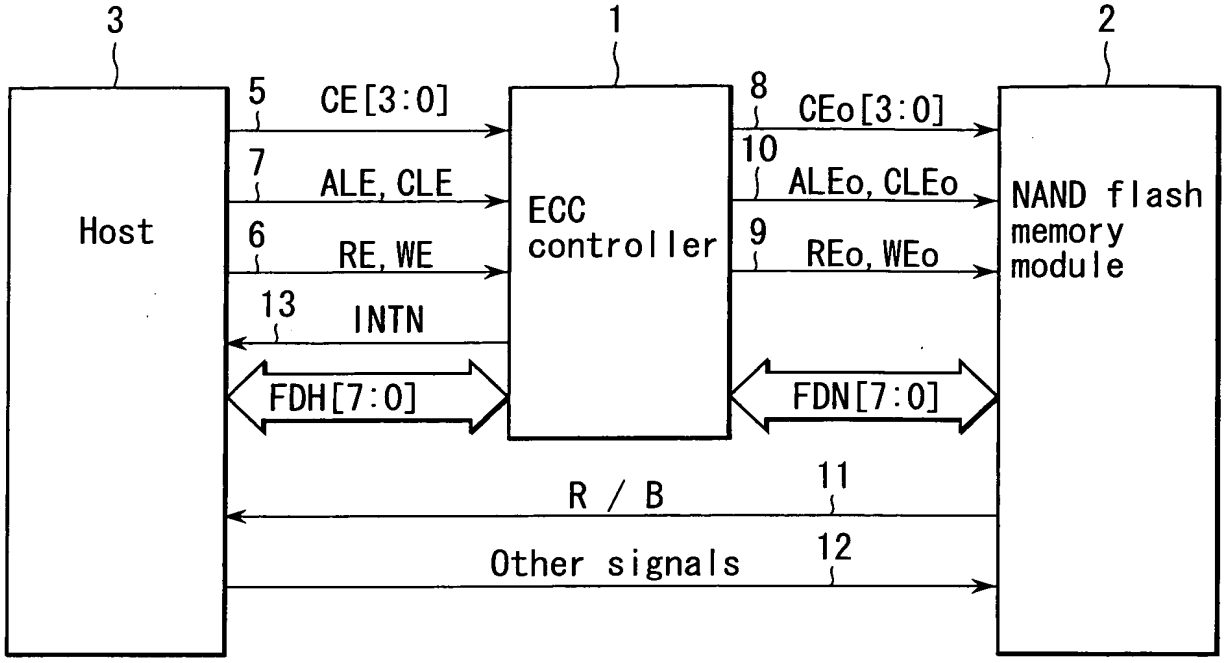
3
1
2
Host
5
CE[3:0]
7
ALE, CLE
6
RE, WE
13
INTN
FDH[7:0]
ECC controller
8
CEo[3:0]
10
ALEo, CLEo
9
REo, WEo
FDN[7:0]
NAND flash memory module
R / B
11
Other signals
12

FIG. 1

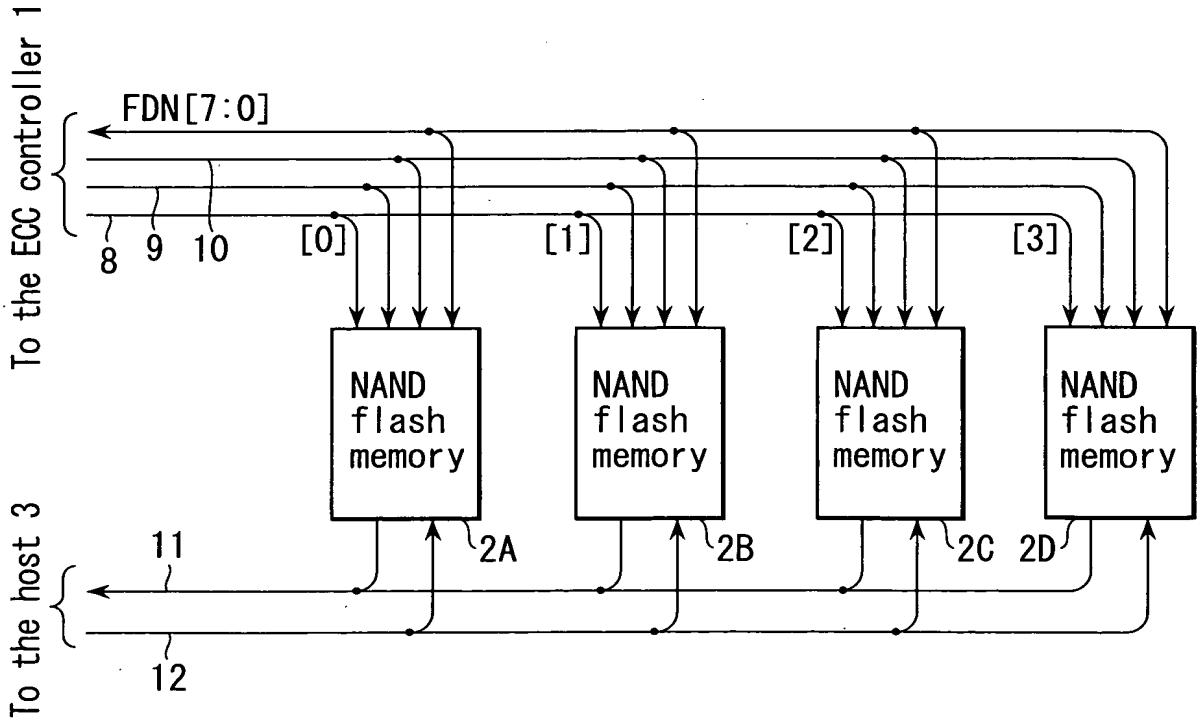
To the ECC controller 1
FDN[7:0]
8
9
10
[0]
[1]
[2]
[3]
NAND flash memory
NAND flash memory
NAND flash memory
NAND flash memory
2A
2B
2C
2D
To the host 3
11
12

FIG. 2

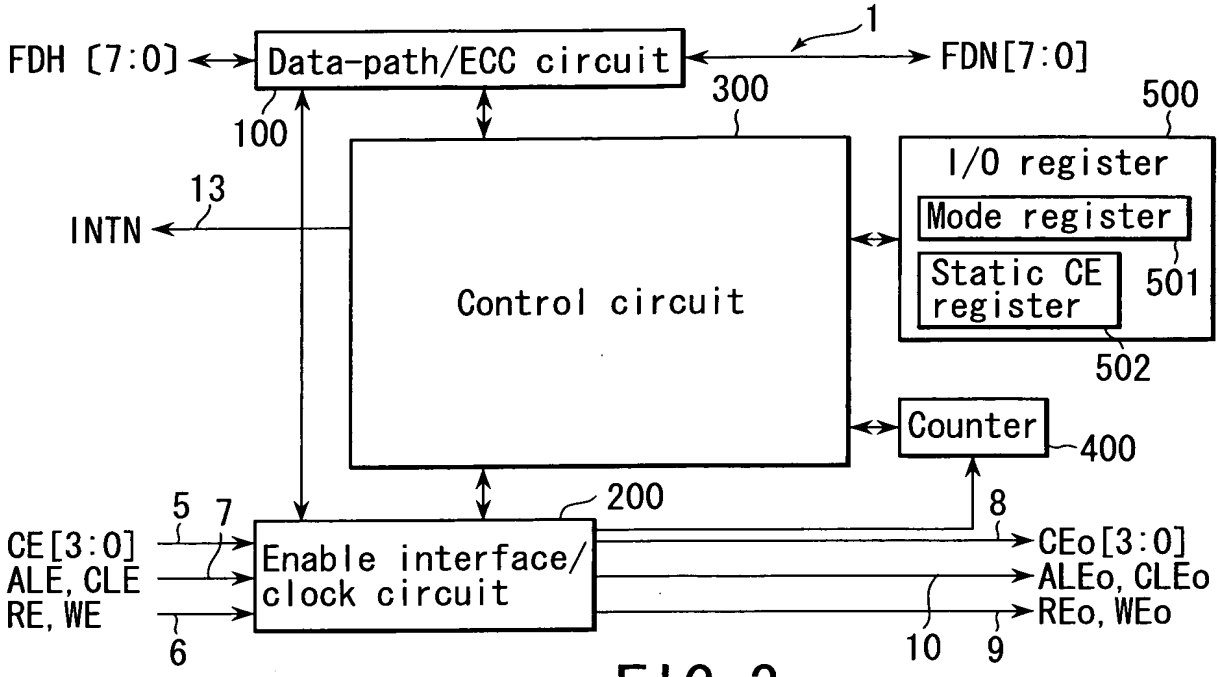
FDH [7:0]
Data-path/ECC circuit
1
FDN[7:0]
100
300
500
I/O register
Mode register
Static CE register
501
502
13
INTN
Control circuit
Counter
400
200
5
7
8
CE[3:0]
ALE, CLE
RE, WE
Enable interface/ clock circuit
CEo[3:0]
ALEo, CLEo
REo, WEo
6
10
9

FIG. 3

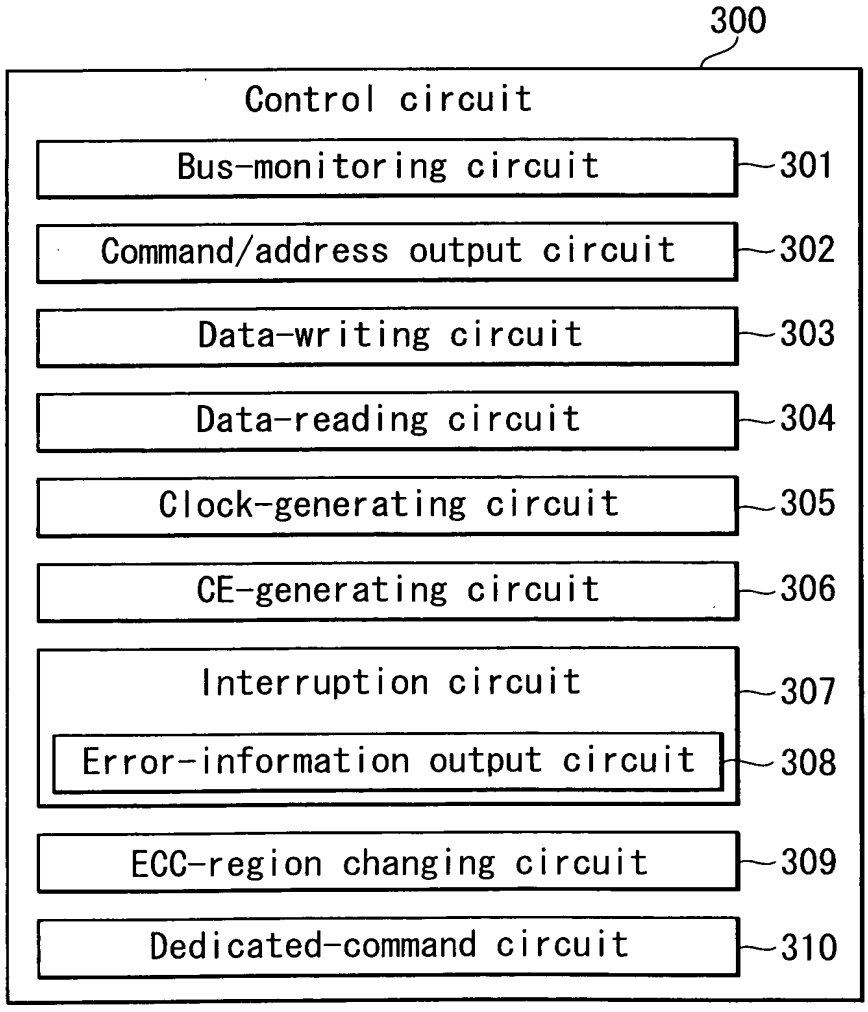
300
Control circuit
Bus-monitoring circuit
301
Command/address output circuit
302
Data-writing circuit
303
Data-reading circuit
304
Clock-generating circuit
305
CE-generating circuit
306
Interruption circuit
307
Error-information output circuit
308
ECC-region changing circuit
309
Dedicated-command circuit
310

FIG. 4

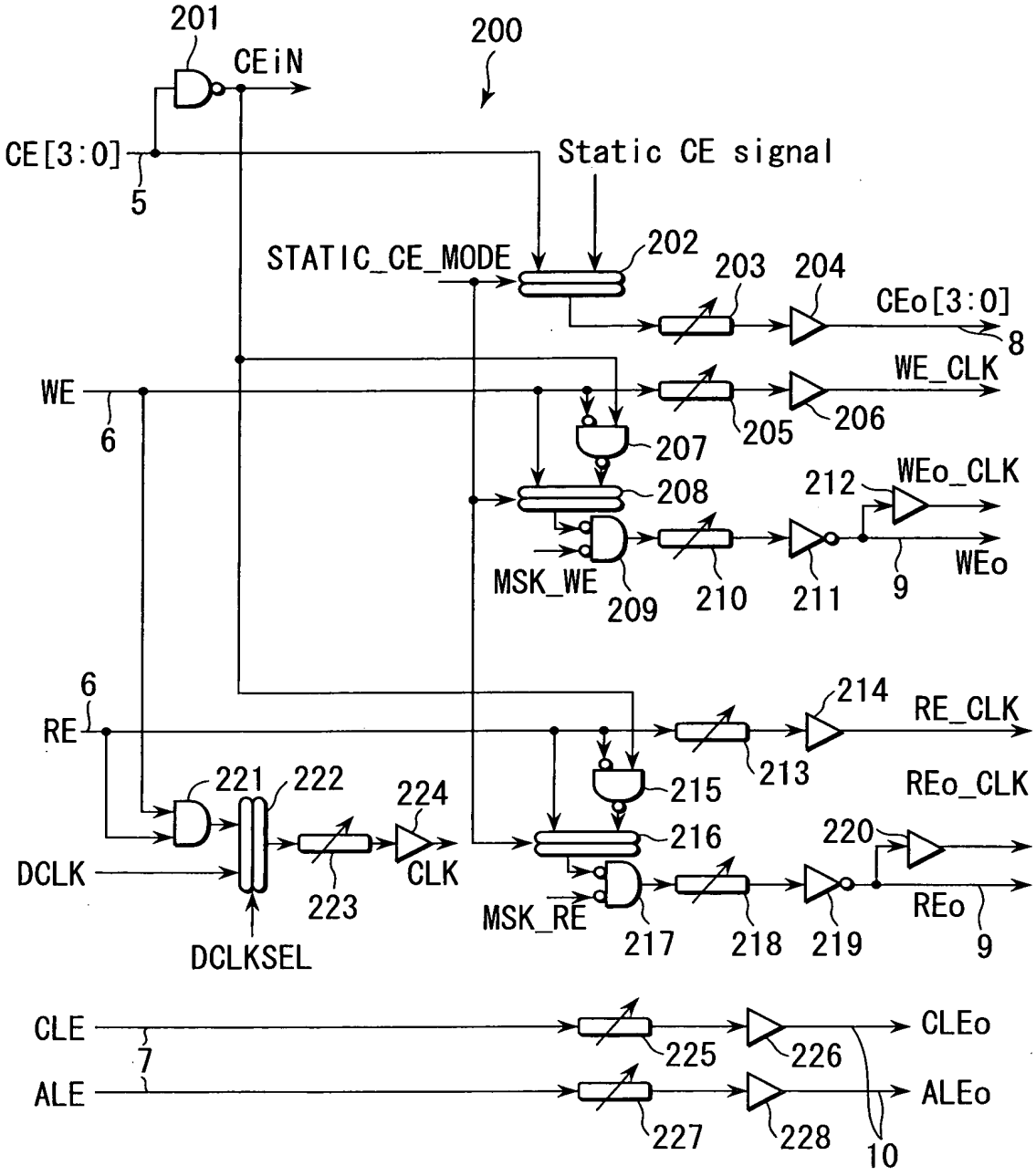
201
CEiN
200
CE[3:0]
5
Static CE signal
STATIC_CE_MODE
202
203
204
CEo[3:0]
8
WE
6
WE_CLK
205
206
207
208
212
WEo_CLK
MSK_WE
209
210
211
9
WEo
6
RE
214
RE_CLK
213
215
REo_CLK
221
222
224
216
220
DCLK
223
CLK
MSK_RE
217
218
219
REo
9
DCLKSEL
CLE
7
225
226
CLEo
ALE
227
228
ALEo
10

FIG. 5

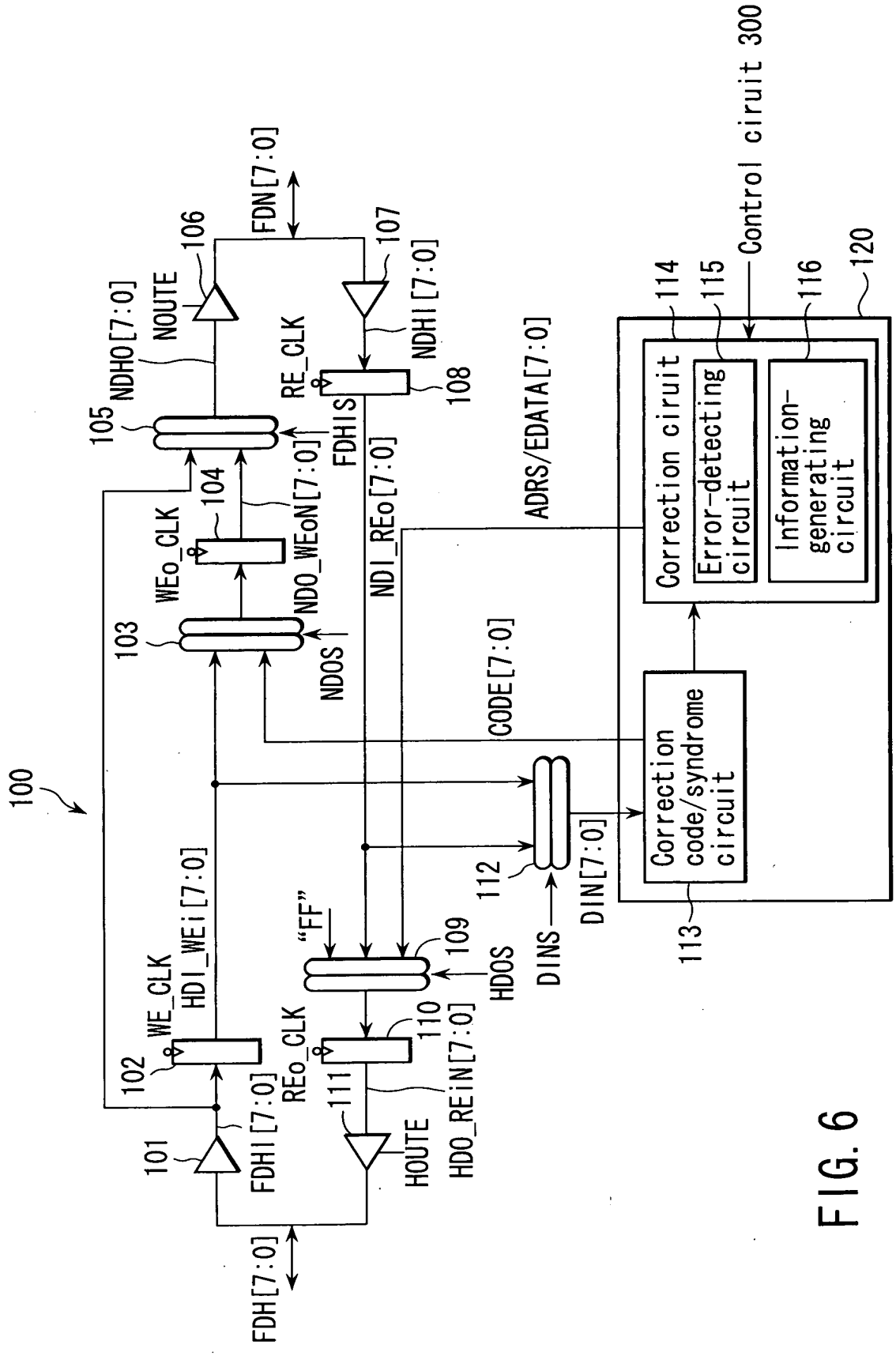
100
FDH[7:0]
101
FDHI[7:0]
102
WE_CLK
HDI_WEi[7:0]
103
WEo_CLK
104
NDO_WEoN[7:0]
105
NDHO[7:0]
NOUTE
106
FDN[7:0]
107
NDHI[7:0]
108
RE_CLK
FDHIS
NDI_REo[7:0]
NDOS
"FF"
109
HDOS
110
REo_CLK
111
HDO_REiN[7:0]
HOUTE
112
DIN[7:0]
DINS
113
ADRS/EDATA[7:0]
CODE[7:0]
Correction code/syndrome circuit
Correction ciruit
Error-detecting circuit
Information-generating circuit
114
115
116
120
Control ciruit 300

FIG. 6

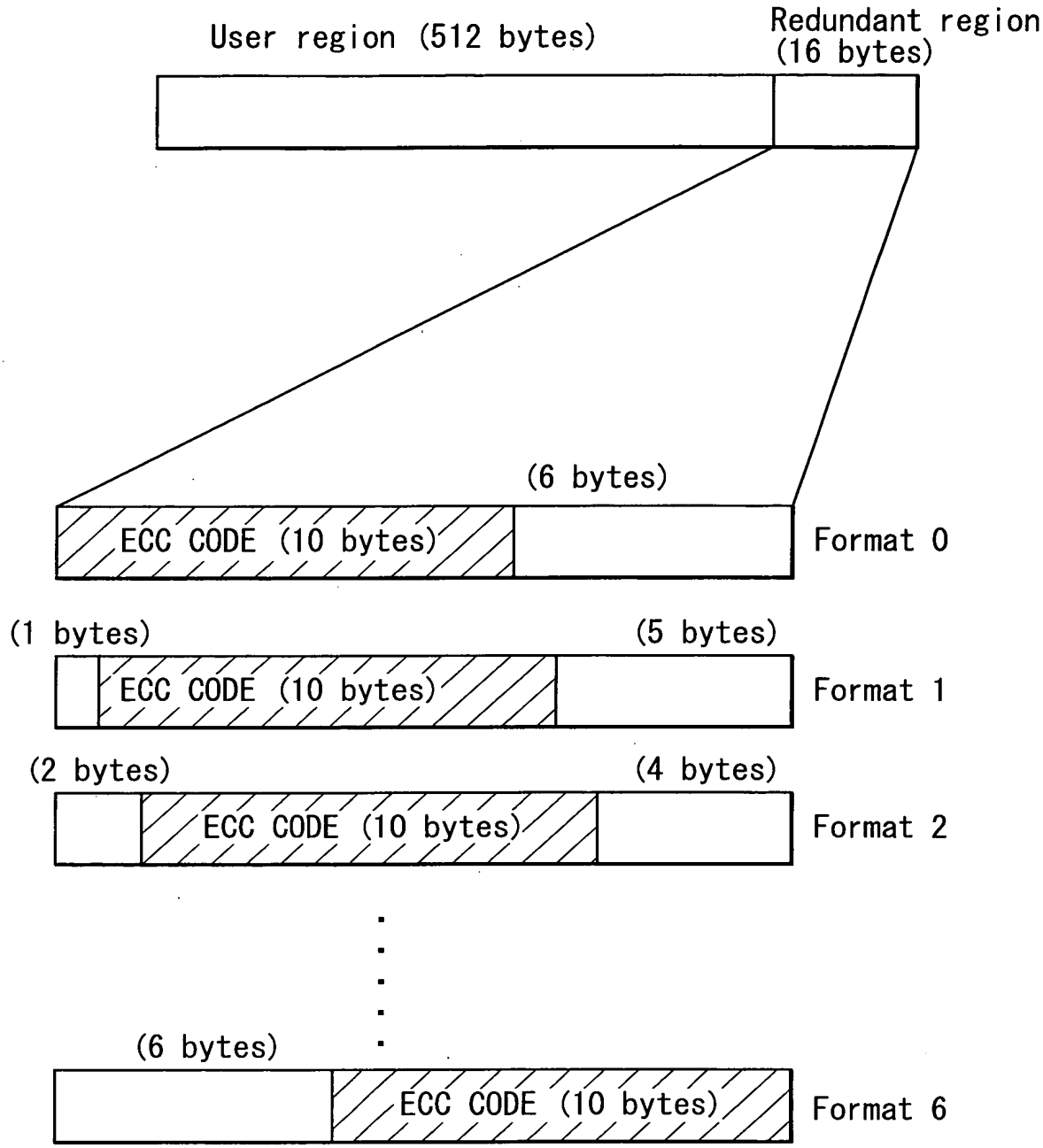
User region (512 bytes)
Redundant region (16 bytes)
(6 bytes)
ECC CODE (10 bytes)
Format 0
(1 bytes)
(5 bytes)
ECC CODE (10 bytes)
Format 1
(2 bytes)
(4 bytes)
ECC CODE (10 bytes)
Format 2
(6 bytes)
ECC CODE (10 bytes)
Format 6

FIG. 7

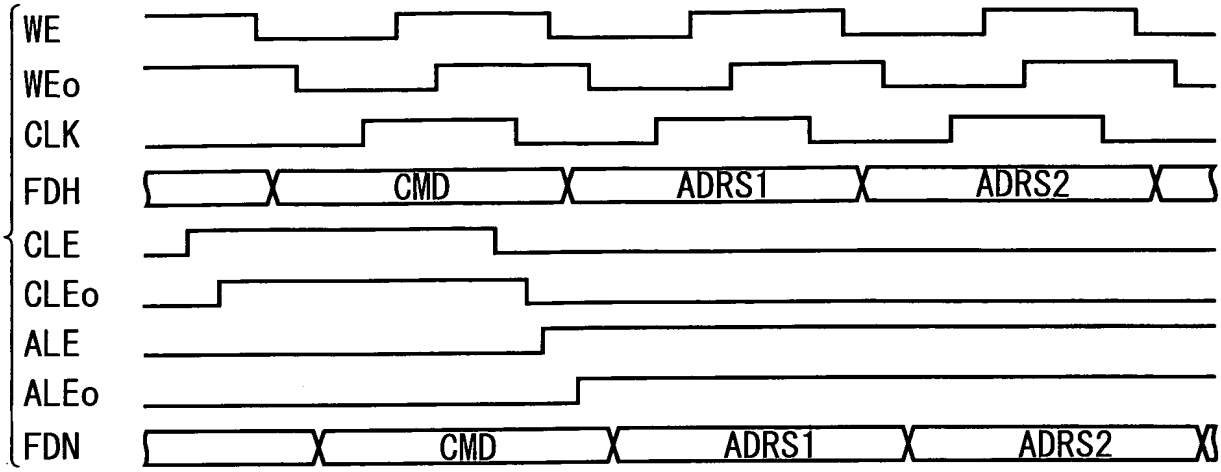

FIG. 8

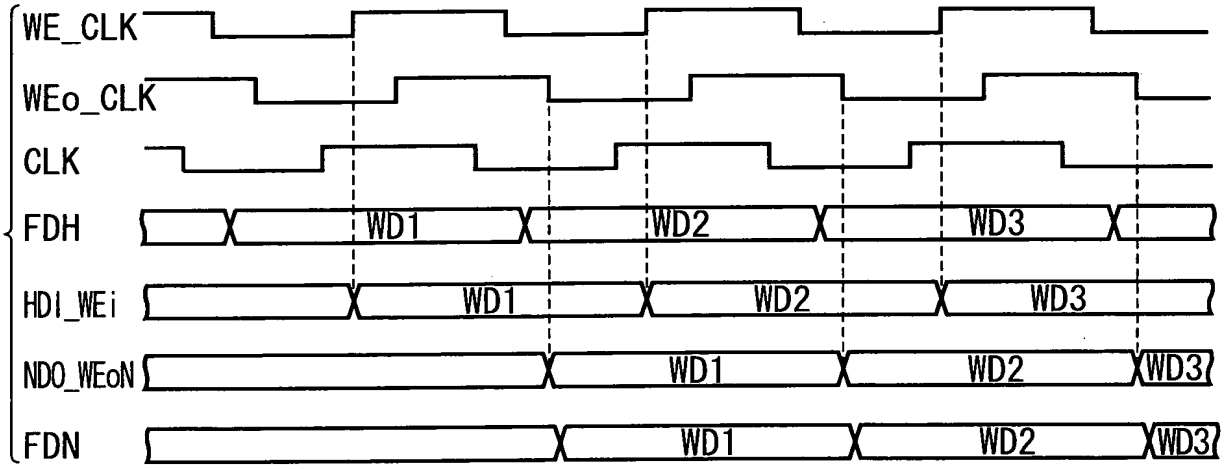

FIG. 9

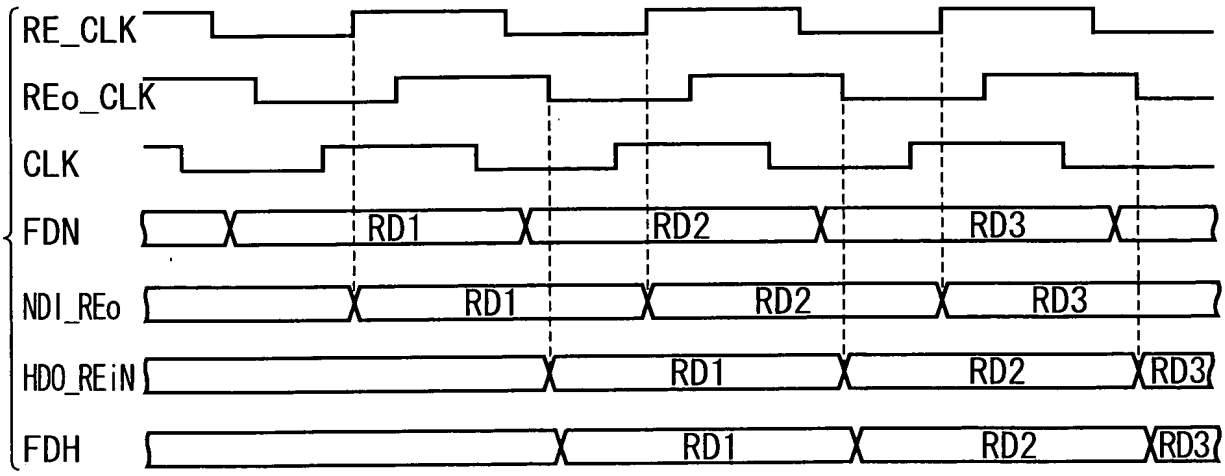

FIG. 10

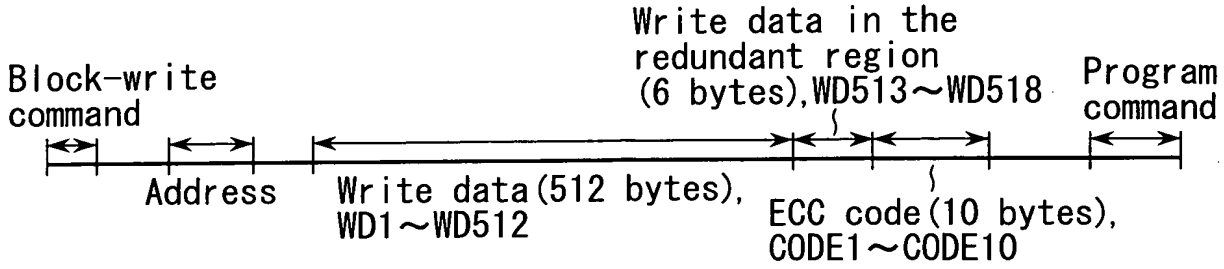

FIG. 11

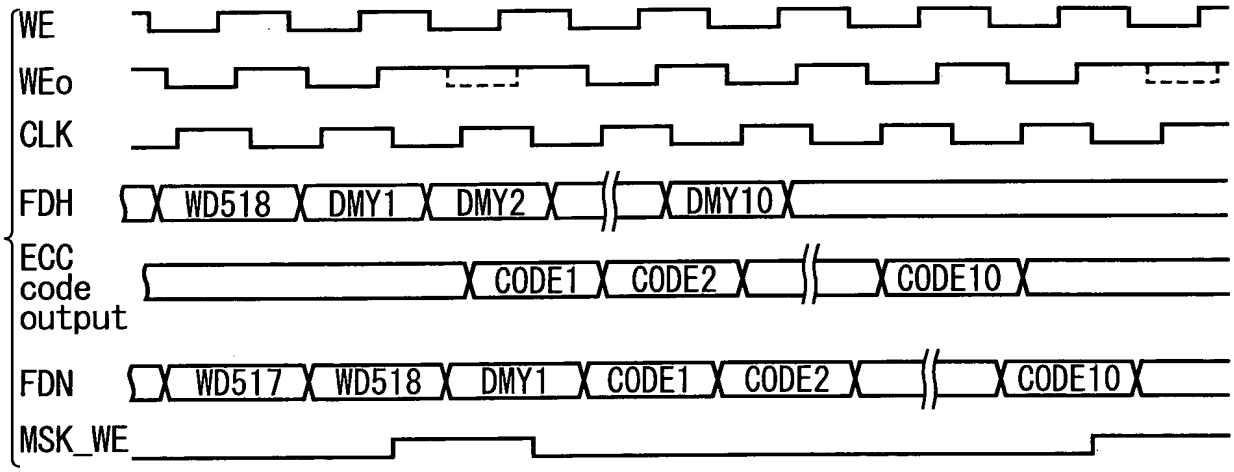

FIG. 12

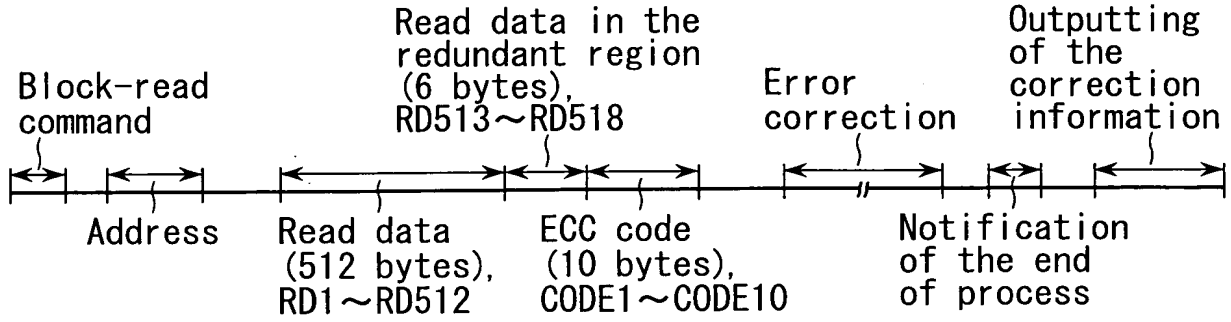

FIG. 13